What is Claimed:

1. A digital filter, comprising:

at least two multiple stage shift registers;

a plurality of multiplier corresponding in number to the number of stages in the at least two multiple stage shift registers, each multiplier receiving as a first input an output from a stage of the at least two multiple stage shift registers, each multiplier producing an output that is a product of inputs thereto:

a tap weight shifter coupled to a top weight source to receive tap weights, the tap weight shifter coupled to provide a second input to each multiplier, the tap weight shifter capable of circularly shifting tap weights; and

an adder for summing the multiplier outputs to provide a sum output.

2. A digital filter as recited in claim 1, further comprising:

a multiplier stage buffer for receiving and storing digital samples, outputs from the multiple stage buffer being coupled to provide inputs to the at least two multiple stage shift registers.

3. A digital filter as recited in claim 2, wherein the multiple stage buffer is a serial-input, parallel-output buffer.

4. A digital filter as recited in claim 1, wherein tap weights received by the tap weight shifter one bit wide.

5. A digital filter as recited in claim 1, wherein tap weights received by the tap weights received by the tap weight shifter are more than one bit wide and having a bit width that is no greater than a bit width of stages of the shift registers.

6. A digital filter as recited in claim 1, wherein the digital filter is implemented in software.

7. A digital filter as recited in claim 1, wherein the digital filter is implemented in an integrated circuit.

8. A digital filter as recited in claim 7, wherein the digital filter is implemented in an application specific integrated circuit.

9. A digital filter as recited in claim 7, wherein the digital filter is implemented in a digital signal processor.

10. A digital filter as recited in claim 7, wherein the digital filter is implemented in a microcontroller.

11. A digital filter as recited in claim 7, wherein the digital filter is implemented a microprocessor.

12. A digital filter as recited in claim 1, further comprising a tap weight source from which to receive tap weights.

13. A digital filter as recited in claim 12, wherein the tap weight source is random access memory.

14. A digital filter as recited in claim 12, wherein the tap weight source is read-only memory.

15. A digital filter as recited in claim 12, wherein the tap weight source is a processor.

16. A receiver including a digital filter comprising:

at least two multiple stage shift registers;

a plurality of multiplier corresponding in number to the number of stages in the at least two multiple stage shift registers, each multiplier receiving as a first input an output from a stage of the at least two multiple stage shift registers, each multiplier producing an output that is a product of inputs thereto:

a tap weight shifter coupled to a top weight source to receive tap weights, the tap weight shifter coupled to provide a second input to each multiplier, the tap weight shifter capable of circularly shifting tap weights; and

an adder for summing the multiplier outputs to provide a sum output.

17. A receiver as recited in claim 16, further comprising:

a multiplier stage buffer for receiving and storing digital samples, outputs from the multiple stage buffer being coupled to provide inputs to the at least two multiple stage shift registers.

18. A receiver as recited in claim 17, wherein the multiple stage buffer is a serial-input, parallel-output buffer.

19. A receiver as recited in claim 16, wherein tap weights received by the tap weight shifter one bit wide.

20. A receiver as recited in claim 16, wherein tap weights received by the tap weight shifter are more than one bit wide and having a bit width that is no greater than a bit width of stages of the shift registers.

21. A receiver as recited in claim 16, wherein the digital filter is implemented in software.

22. A receiver as recited in claim 16, wherein the digital filter is implemented in an integrated circuit.

23. A receiver as recited in claim 22, wherein the digital filter is implemented in an application specific integrated circuit.

24. A receiver as recited in claim 22, wherein the digital filter is implemented in a digital signal processor.

25. A receiver as recited in claim 22, wherein the digital filter is implemented in a microcontroller.

26. A receiver as recited in claim 22, wherein the digital filter is implemented a microprocessor.

27. A receiver as recited in claim 16, further comprising a tap weight source from which to receive tap weights.

28. A receiver as recited in claim 27, wherein the tap weight source is random access memory.

29. A receiver as recited in claim 27, wherein the tap weight source is read-only memory.

30. A receiver as recited in claim 27, wherein the tap weight source is a processor.

31. A receiver as recited in claim 16, wherein the receiver is a handset.

32. A receiver as recited in claim 16, wherein the receiver is a base station.

33. A method of filtering digital data, comprising the steps of:

a. shifting digital data into first and second multiple stage shift registers;

b. multiplying an output from each stage of the first and second multiple stage shift registers by an associated, respective tap weight to produce a plurality of products;

c. combining the plurality of products to form a sum

d. circularly shifting the tap weights; and

e. repeating steps b and c.

34. A method of filtering digital data as recited in claim 33, further comprising the step of

shifting digital data into registers of a buffer prior to shifting the digital data into first and second multiple stage shift registers.

35. A method of filtering data, comprising the steps of:

a. shifting data into N multiple stage shift registers, each of the N multiple stage shift registers having at least L stages, N and L being integers, N being at least 2;

b. multiplying an output from each of the at least L stages of the N multiple stage shift registers by a corresponding tap weight to produce a plurality of products;

c. combining the plurality of products to form a sum;

d. circularly shifting the tap weights;

e. repeating steps b, c, and d N-2 times;

f. repeating steps b and c again.

36. A method of filtering data, further comprising the steps of following step f, repeating steps a through f.

37. A method of filtering data as recited in claim 35, further comprising the step of shifting N pieces of data into registers of a buffer for temporary storage prior to shifting the N pieces of data into respective ones of the N multiple stage shift registers.